C. Remarks

Rejections Under 35 U.S.C. §112, Second Paragraph.

The claims have been amended to address this ground for rejection.

Rejection of Claims 1-3 and 5-6 Under 35 U.S.C. §102(b) based on *Kaya et al.* (U.S. Patent No. 5,821,581).

The invention of amended claim 1 is directed to an insulated gate field effect transistor that includes a first source/drain area, a second source/drain area, and a gate electrode structure formed on a gate insulating film. The gate insulating film includes a first gate insulating film formed on a first channel area portion and a second gate insulating film formed on a second channel area portion. The gate electrode structure is formed on a gate insulating film formed on a channel area disposed between the first source/drain area and the second source drain area. A second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area when viewed from the gate structure. In addition, the gate electrode structure includes a first gate electrode and a second gate electrode electrically connected through a third gate electrode.

As is well established, anticipation requires the presence of a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention.[1]

The cited reference does not show, nor can suggest, a first gate electrode and second gate electrode that are "electrically connected through a third gate electrode". The reference *Kaya et al.* is directed to a non-volatile split-gate memory cell that includes a control gate (22) (argued to correspond to Applicants' first gate electrode) as well as a ***floating*** gate (18) (argued to correspond to Applicants' second gate electrode). However, in *Kaya et al.* the control gate is not electrically connected to the floating gate, but rather intentionally insulated from the floating gate:

> [C]ontrol gate 22 is separated from the floating gate 18 by insulation layer 24... (*Kaya et al.*, Col. 3, Lines 47-48).

[1] Scripps Clinic & Research Found. v. Genetech Inc., 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

As would be well understood by those skilled in the art, electrically connecting a floating gate to a corresponding control gate would defeat the entire purpose of the device, as the floating gate would no longer be "floating" and could not modify a resulting threshold voltage.

Accordingly, the cited reference does not show all the limitations of amended claim 1, and this ground for rejection is traversed.

Amended claim 3, which depends from claim 1, is believed to be separately patentable over the cited reference. Claim 3 now clarifies the "sidewall configuration" of the first and second gate electrodes, emphasizing that these gate electrodes are "generally parallel with one another in a direction perpendicular to the gate insulating film".

The control gate and floating gate of *Kaya et al.* appear to have the opposite orientation, being parallel to one another in a direction parallel (and not perpendicular) to a FAMOS gate oxide 20 and pass oxide 26 (argued to correspond to Applicant's gate insulating film).

For this reason, claim 3 is believed to include additional limitations not shown or suggested by the cited reference, and so is separately patentable.

Rejection of Claims 1 and 4 Under 35 U.S.C. §102(b) based on *Lee* (U.S. Patent No. 5,600,168).

As noted above, amended claim 1 includes the limitation of a gate electrode structure that is formed on a gate insulating film formed on a channel area disposed between the first source/drain area and the second source drain area. A second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area when viewed from the gate structure.

*Lee* shows a MOS transistor with first, second, and third conduction layers (argued to correspond to Applicant's gate electrode structure) formed between a source and drain that each includes a low density impurity region 24 and a high density impurity region 26. However, the source and drain of *Lee* do not have different impurity concentration distributions, particularly when viewed from the gate structure. Rather, the source and drain of the reference are essentially identical, being formed with the same ion implantation steps.[2]

Accordingly, because the reference is not believed to show or suggest all the limitations of claim 1, this ground for rejection is traversed.

[2] See *Lee*, FIGS. 4f and 4g. The same ion implantation steps form low density impurity regions and high density impurity regions for the source and drain.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Rejection of Claims 7 and 8 Under 35 U.S.C. §103(a), based on *Kaya et al*.

Claim 7, which depends from claim 1, recites that a capacitor is connected to the first source/drain area and a bit line is electrically connected to the second source/drain area.

As is well settled, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art.

The rejection notes that the cited reference does not disclose a capacitor as recited in claim 7. To show such a feature, the rejection proposes modifying the reference according to the following reasoning:

> Kaya does not explicitly disclose a capacitor electrically connected to the first source/drain area, however, this is a common configuration which was well known... and would therefore have been obvious... (Office Action, dated 02/07/2007, Page 6, Second full paragraph).

Applicant must strenuously disagree with this reasoning. It is noted that *Kaya et al.* discloses a non-volatile memory cell. This memory cell relies on the charge of a floating gate to retain a data value. Applicant does not believe incorporating a capacitor into such a cell, or such types of cells, would be obvious, and would likely render the invention non-functional. In particular, it is not understood how the memory cell of *Kaya et al.* could be programmed or erased if a capacitor is couple to a source or drain.

Accordingly, Applicant believes a prima facie case of obviousness has not been established. The above motivation/suggestion for modifying the non-volatile memory cell of *Kaya et al.* cannot be from the reference itself, as such modification would change the principle operation of the device or render it nonfunctional.

If the rejection is taking official notice with respect to such reasoning, Applicant seasonably traverses and requests a reference in support. Such a reference should demonstrate how it would be obvious to incorporate a capacitor with a split gate nonvolatile memory cell, such as that shown in *Kaya et al.*

For these reasons, this ground for rejection is traversed.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Claims 1 and 3 have been amended. Claim 4 has been cancelled.

The present claims 1-3 and 5-9 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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